Amendments to the Claims:

1. (Currently Amended) A BISR scheme comprising:

a fuse controller;

a plurality of memories connected to the fuse controller;

a plurality of fuse blocks connected to the fuse controller, said BISR scheme configured such that said memories share said fuse blocks, said BISR scheme configured to perform a wafer sort.

2. (Original) A BISR scheme as recited in claim 1, wherein the memories are serially connected to the fuse controller.

3. (Original) A BISR scheme as recited in claim 1, wherein the fuse blocks are serially connected to the fuse controller.

4. (Original) A BISR scheme as recited in claim 1, wherein the memories are serially connected to the fuse controller and the fuse blocks are serially connected to the fuse controller.

5. (Original) A BISR scheme as recited in claim 1, wherein there are more memories than fuse blocks.

6. (Currently Amended) A BISR scheme as recited in claim 1, wherein ~~there~~ the fuse controller is configured to program memory addresses into the fuse blocks.

7. (Currently Amended) A BISR scheme as recited in claim 1, wherein ~~there~~ the fuse controller is configured to program memory addresses and repair solutions into the fuse blocks.

8. (Currently Amended) A method of implementing a BISR scheme comprising:

providing a fuse controller, a plurality of memories connected to the fuse controller, and a plurality of fuse blocks connected to the fuse controller; and

having the memories share the fuse blocks, further comprising performing a wafer sort.

9. (Canceled)

10. (Original) A method as recited in claim 8, further comprising burning the fuse blocks to program a repair solution and memory addresses.

11. (Original) A method as recited in claim 10, further comprising loading the repair solution and memory addresses into the fuse controller.

12. (Original) A method as recited in claim 8, further comprising loading fuse values into the fuse controller.

13. (New) A BISR scheme comprising:

a fuse controller;

a plurality of memories connected to the fuse controller;

a plurality of fuse blocks connected to the fuse controller, said BISR scheme configured such that said memories share said fuse blocks, wherein the memories are configured in a serial chain, wherein one of the memories is connected to the fuse controller and the other memories are serially connected to each other and to the memory which is connected to the fuse controller.

14. (New) A BISR scheme as recited in claim 13, wherein the fuse blocks are configured in a serial chain, wherein one of the fuse blocks is connected to the fuse controller and the other fuse blocks are serially connected to each other and to the fuse block which is connected to the fuse controller.

15. (New) A BISR scheme as recited in claim 13, wherein there are more memories than fuse blocks.

16. (New) A BISR scheme as recited in claim 13, wherein there fuse controller is configured to program memory addresses into the fuse blocks.

17. (New) A BISR scheme as recited in claim 13, wherein there fuse controller is configured to program memory addresses and repair solutions into the fuse blocks.

18. (New) A BISR scheme as recited in claim 13, wherein the BISR scheme is configured to perform a wafer sort.

19. (New) A method of implementing a BISR scheme comprising:

providing a fuse controller, a plurality of memories connected to the fuse controller, and a plurality of fuse blocks connected to the fuse controller; and

having the memories share the fuse blocks such that the memories are configured in a serial chain, wherein one of the memories is connected to the fuse controller and the other memories are serially connected to each other and to the memory which is connected to the fuse controller.

20. (New) A method as recited in claim 19, further comprising providing that the fuse blocks are configured in a serial chain, wherein one of the fuse blocks is connected to the fuse controller and the other fuse blocks are serially connected to each other and to the fuse block which is connected to the fuse controller.

21. (New) A method as recited in claim 19, further comprising providing that there are more memories than fuse blocks.

22. (New) A method as recited in claim 19, further comprising burning the fuse blocks to program a repair solution and memory addresses.

23. (New) A method as recited in claim 22, further comprising loading the repair solution and memory addresses into the fuse controller.

24. (New) A method as recited in claim 19, further comprising loading fuse values into the fuse controller.

25. (New) A method as recited in claim 19, further comprising performing a wafer sort.